Published at EPE 2005 - European Conference on Power Electronics and Applications - www.epe2005.com

Addressing the Topologies, Converters, and Switching Devices for Intermediate Bus Architectures

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ABSTRACT

The distributed voltage in Intermediate Bus Architectures (IBAs) is by no means standardized in the power electronics industry. This paper investigates the efficiency of both the front-end converter and the point-of-load (POL) converter commonly used in IBAs, when implemented with various distributed voltage levels and MOSFETs with different device parameters.

BACKGROUND

With power demands increasing in all the markets served by the electronics industry—consumer, computer, automotive and telecom—power supply designers have been compelled to re-evaluate conventional circuit topologies. The development of the IBA came as a result. However, the industry has yet to standardize on a specific voltage level for IBAs. Instead, this varies from design to design, and system engineers must choose the best level for their application based on several factors. For example, where the main system circuit board requires 3.3 V or 5 V for logic circuits, it makes sense to have a distributed bus that supplies these voltages and is then converted to the lower core voltages at the point of load. In the near future, however, these voltage requirements will reduce even further, and the voltages for the logic circuits will be in the region of 2.5 V, a level too low to support a distributed bus. This gives circuit designers a new opportunity to choose and determine the ideal voltage for the distributed bus, and this paper goes some way to aid that decision.

INTRODUCTION

Point-of-load (POL) converters have emerged as a popular solution for applications whose circuits require voltages of 3.3 V and below. The demand for these types of voltage levels stems from the requirement for lower core voltages, and it is obvious that the current requirements for these converters will increase even if the power capability stays the same. These low voltages and high currents are forcing the power conversion industry to re-evaluate conventional circuit topologies, component selection, and packaging concepts.

The POL requirement originally arose from computer hardware developments, but it is now being seen throughout the electronics industry wherever any level of intelligence is required. Feature-rich applications and circuits with added functionality that use devices such as DSPs, ASICs, and microcontrollers are driving power requirements higher and thus creating a need for more complex power supplies. POL circuits are especially being implemented in telecom base stations and the network infrastructure.

Since the introduction of the POL concept, many different configurations have been suggested and used, and currently there does not appear to be one fixed strategy for stepping down high voltages, such as 48 V, to voltages as low as 0.9 V. In the past, traditional distributed power architectures (DPA - Figure 1) were used to supply all the required voltage levels from a single “front-end converter.” In fixed-telecom applications, the input voltage of 48 V would be stepped down, with transformer isolation, to several different voltage outputs and distributed throughout the card or subsystem to the sub-circuit requiring the power. In some cases this would result in high currents being circulated around the PCB, causing large voltage drops, increased power consumption, large PCB tracks, and poor regulation. The IBA solution (Figure 2) is essentially a two-step conversion process. The first part is similar to the DPA, with a front-end converter and the second step converter taking the distributed bus voltage and converting it to the required voltage level at the point where the system requires the power.

The paper explores front-end converter topologies, along with POL converters, synchronous rectification, and the appropriate controllers and devices necessary to implement these converters. Using various semiconductor switches, specifically designed for these topologies, efficiency measurements are made and an objective assessment of these topologies in several applications and power ranges is given.

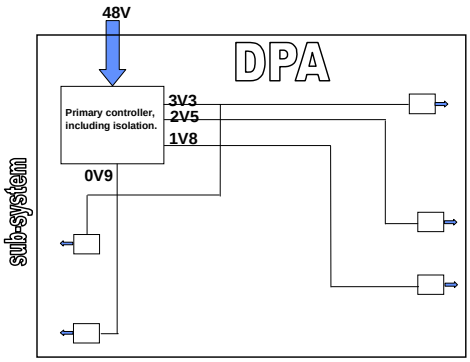

Figure 1. Block diagram showing typical architecture of a single front-end converter supplying all the voltage levels.

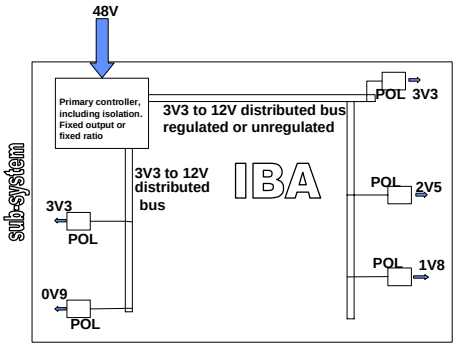

Figure 2. Block diagram showing typical architecture of a point-of-load distributed bus power system.

THE FRONT-END CONVERTER

The front-end controller performs several functions, including a large step-down ratio and galvanic isolation. The entire power throughput will have to pass through the front-end converter and conversely through the isolating transformer. In some circumstances this may be an 'off the shelf' voltage regulator module (VRM), a custom module, or a discrete version designed in-house. Whichever route the manufacturer takes, the topology is usually determined by the power requirements of the system. The front-end converter must be very efficient, since all the power for the sub-system passes through it and any inefficiency will be transferred through to the end output.

Table 1 outlines a few of the available topologies that can be used in the front-end converter. The performance of two of the most popular topologies (forward and half-bridge) is examined and the paper presents efficiency results for different output voltages.

	Common Characteristics				
Topology	**Power Level [W]**	**Voltage Stress [V]**	**Output Ripple Freq [Hz]**	**Max. Duty Cycle**	**Relative Cost**
Flyback	5 -150	$V_{in}+(N_p/N_s)V_{out}$	f_s	<0.5	Low
Forward Resonant Reset	10 – 250	$2\times V_{in}$	f_s	<0.5	Low
Forward Active Clamp Reset	10 – 250	$2\times V_{in}$	f_s	<0.5	Low-Med
Push-Pull	15-150	$2\times V_{in}$	$2\times f_s$	<1.0	Med
Half Bridge	50-400	V_{in}	$2\times f_s$	<1.0	Med
Full Bridge	200-2k	V_{in}	$2\times f_s$	<1.0	High

Table 1. Characteristics of common converters.[1]

The Forward Converter

The forward converter is very similar to the step-down dc-to-dc converter, with the transformer providing galvanic isolation, rather than being used to store energy. For the topology investigated in this paper, a simple reset winding is included to reset the magnetizing current in the transformer to prevent core saturation. The circuit used is a self-resonant reset circuit, which resets the magnetizing current and also recovers this magnetizing energy by charging it back to the input. This topology also allows for a large ratio of input to output voltages.

The controller used is a Vishay Siliconix Si9118DY, and for simplicity the readily available 25-W demo-board[1] is used to evaluate a range of devices with varying parameters. Although the target requirement would be a higher power level, the circuit allows a valid comparison of several switching devices. This demo board is used

to determine the performance of distributed buses, from an output voltage of 12 V to 3.3 V. To obtain the range of outputs the demo board[1&2] was altered slightly; this included altering the number of turns on the transformer, changing the feedback resistors, and using higher-voltage output capacitors. The schematic of the circuit is shown in Figure 3.

Four devices were chosen for evaluation, with different on-resistances and capacitances. The parameters of these devices are shown in Table 2. The devices are listed in ascending order of $r_{DS(on)}$, with devices 1 and 2 having similar dynamic parameters to each other and devices 3 and 4 having similar switching characteristics, but less than those of 1 and 2.

Device Number	Device Name	Voltage rating [V]	$r_{DS(on)}$ (Ω)	Q_g (nc)	Q_{gd}/Q_{gs} ratio
1	Si4490DY	200	0.08	34	1.6
2	Si4434DY	250	0.155	34	1.5
3	Si4464DY	200	0.24	12	1.5
4	Si9422DY	200	0.42	13	0.7

Table 2. Devices chosen for evaluation.

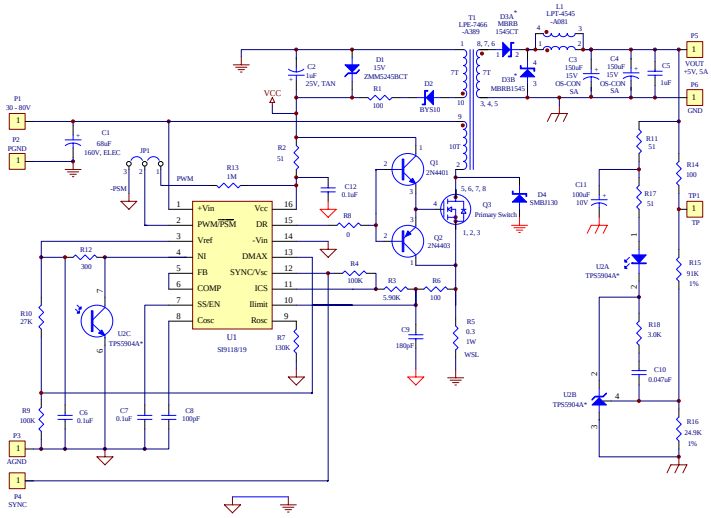

Figure 3. Circuit schematic of the front-end forward converter.[1&2]

Three different output voltages were chosen for comparison, these being 3.3 V, 5 V and 12 V. Figure 4 shows the efficiencies for devices for the 5-V output, with load currents from 1 A to 5 A, giving a maximum power output of 25 W. It can be seen that when the load current reaches 4 A, the devices with the lower $r_{DS(on)}$ (Si4490DY and Si4434DY) start to become more efficient. At the lower current levels the devices with the better switching parameters (Si9422DY and Si4464DY) perform better in terms of efficiency, indicating that the switching losses are the dominant power loss below 4 A. In the case of all four devices, there appears to be a point at approximately 4 A output where the $r_{DS(on)}$ becomes the dominant loss. However, up to 5 A output, the Si4464DY still outperforms the Si4434DY, which has a significantly lower $r_{DS(on)}$ than that of the Si4464DY.

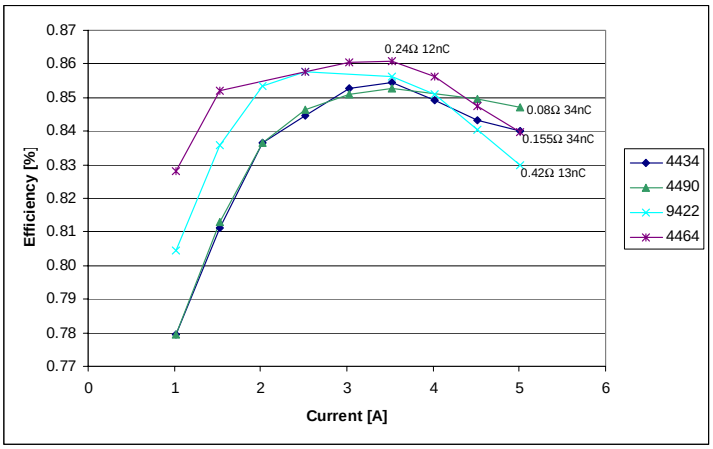

Figure 4. Efficiency results for the Forward converter with a 5V output.

Figure 5 shows the output efficiencies for the two devices which have the lowest $r_{DS(on)}$ and best switching performance combination, devices 1 and 3, for 3.3-V, 5-V and 12-V voltage outputs. These two devices were chosen because they gave the best performance across the load range in the 5-V output converter. For the 3.3-V output, the point at which the low $r_{DS(on)}$ device becomes more efficient is 7 A. In the case of the 12-V output, the lower-$r_{DS(on)}$ device has a higher efficiency at loads of 1.5 A and above. Figure 7 shows that for power levels below 25 W, the 5-V converter is the most efficient. However, the trend indicates that above 25 W, the 12-V bus would be more efficient.

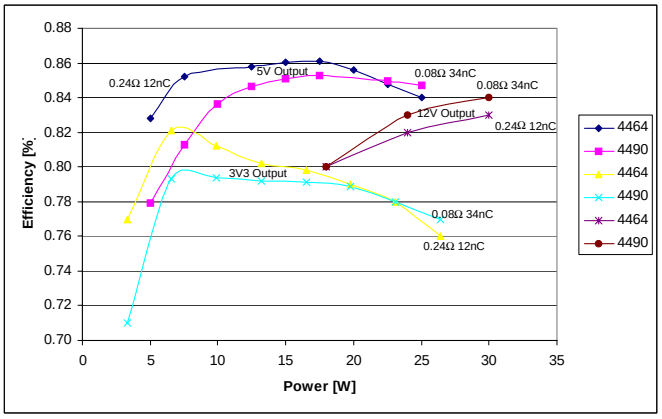

Figure 5. Efficiency results for 3.3-V, 5-V and 12-V outputs.

Figures 6 and 7 show the idealized waveforms for the front-end forward converter at different operating conditions, and these waveforms are used to help describe the efficiency differences under various operating conditions. Figure 6 shows the voltage and current waveforms for the 12-V output converter. With an input voltage of 48 V, the duty cycle will be approximately 36%, giving a primary peak current of nearly 1.8 A for a 2.5-A secondary output. Figure 7 shows the waveforms for the 3.3-V output converter. With this output, the duty cycle is reduced. At the same power level, furthermore, the rms currents are higher, and the peak currents are higher than in the 12-V converter. Therefore, the efficiency of a standard front-end converter improves with a higher output voltage. However, as the bus voltage is increased, the POL converter will be affected as described later in the paper.

It should also be noted that a reduction in duty cycle reduces conduction losses, but increase switching losses.

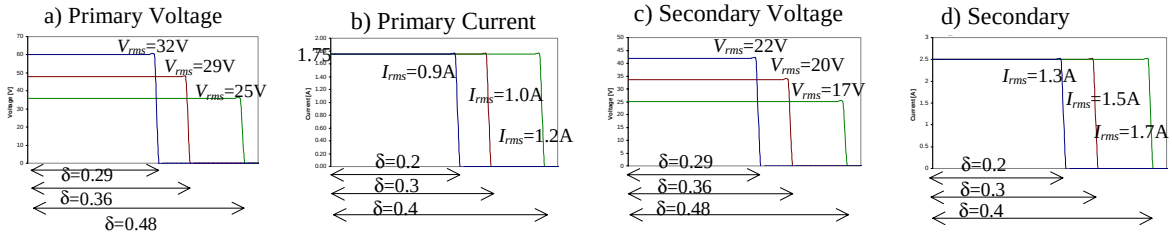

Figure 6. Idealized current and voltage waveforms for 12-V and 2.5-A output
Key δ=0.29 Vin 60 V; δ=0.36 Vin 48 V; δ=0.48 Vin 32 V

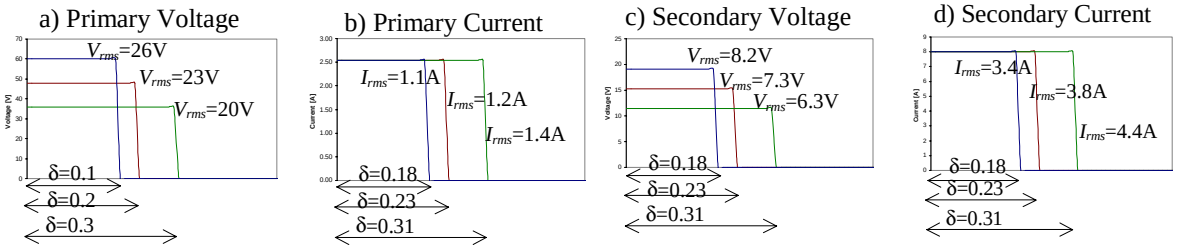

Figure 7. Idealized current and voltage waveforms for 3.3-V and 8-A output.
Key δ=0.18 Vin 60 V; δ=0.23 Vin 48 V; δ=0.31 Vin 32 V

Secondary synchronous rectification

Conduction losses in the secondary-side rectifier diodes are among the factors which affect the efficiency of the front-end converter at higher load currents. Therefore these diodes can be replaced with MOSFETS to reduce the *IV* losses. Self-driven secondary synchronous rectification is relatively simple to achieve with forward converters and is shown in Figure 8. However, care must be taken with the voltage levels that appear on the secondary side transformer. For example, if you consider the ideal voltage across the secondary transformer (Figure 6) for the 12-V converter, the minimum voltage is 25 V. However, with voltage overshoots, this voltage often exceeds 30 V. In this case separate drivers (or separate drive transformers) would be required to be able to control the gate voltage level. Therefore, synchronous rectification was not considered for the 12-V converter. Also since the current levels in the 12-V converter are considerably lower than the 3.3-V converter, the benefits of introducing synchronous rectification are not as great.

A brief investigation of the 3.3-V converter with self-driven synchronous rectification was completed with an input voltage of 36 V, due to the secondary side voltage being below 20 V (the maximum gate source voltage allowed for these devices). Therefore the Si4888DY was used as the MOSFET for synchronous rectification, which offers a good combination of Q_g and $r_{(DS)on}$. Another option is to use a Schottky in parallel with the synchronous MOSFET, to improve the reverse recovery characteristics. An advantage of this is that the Schottky can have a greatly reduced current capability, as it will only be conducting for a small amount of the time.

The efficiency results for the 3.3-V converter, with device 1 from table 2 as the primary switch, are shown in Figure 9. As can be seen the synchronous MOSFETs give greatly improved performance, making this converter more comparable to the higher voltage output converters.

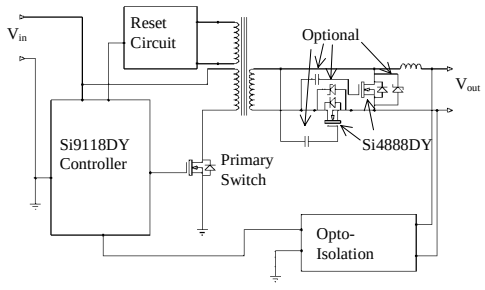

Figure 8. Schematic of the self-driven synchronous rectification

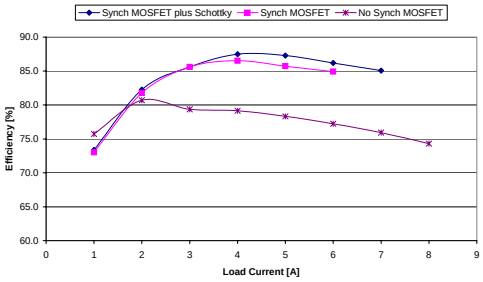

Figure 9. Efficiency results for 3.3 V with Si4490DY primary switch and 36-V input.

The Half-Bridge Converter[3]

The half-bridge dc-to-dc converter configuration consists of two large, equal capacitors connected in series across the dc input, providing a constant potential of ½ V_{in} at their junction, as shown in Figure 10. The MOSFET switches *SW1* and *SW2* are turned on alternatively and are subjected to a voltage stress equal to that of the input voltage. With the capacitors providing a mid voltage point, the transformer sees a positive and negative voltage during switching, resulting in twice the desired peak flux value of the core, since the transformer core is operated in the first and third quadrant off the B-H loop, and experiences twice the flux excursion, for a similar forward converter core. One of the challenges of the past was to develop the synchronous rectifier gate drive logic to enable the synchronous MOSFETs to operate without shoot-through and during long dwell times. The device[3] used in this instance incorporates the synchronous rectifier logic drivers to over come these issues. Figure 11 shows the efficiency results for the half bridge converter with synchronous rectification. Due to the ability to use lower rated V_{DS} parts than the forward converter, the efficiencies are considerably greater. In this case, a device (Si7456DP) with an $r_{DS(on)}$ of 25 mΩ and a gate charge of 36 nC was used. This circuit was designed for power levels up to 60 W.

As can be seen from the from Figure 11, the efficiencies from 4 A to 12 A load output are greater than 90%, giving a greater efficiency level than that achieved with the forward resonant clamp converter.

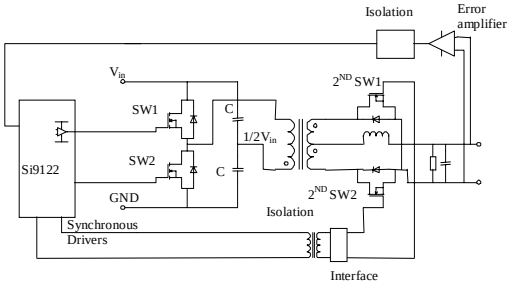

Figure 10. Schematic of the half-bridge dc-to-dc converter.[2]

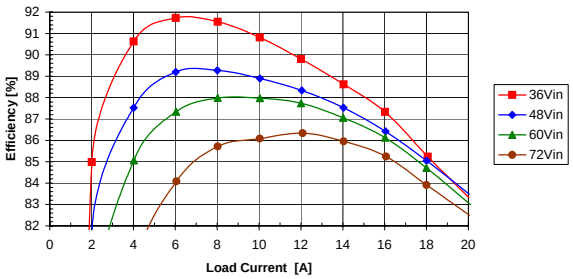

Figure 11. Efficiency results for 3.3 V with Si4490DY primary switch and 36-V input.

THE POL CONVERTER.

Having investigated the possible front-end converters to be used in a distributed bus, we now turn to the requirements of the POL converter, which must have several key characteristics. Firstly, it does not need to be isolated, as the front-end converter has achieved this. Secondly, depending on the required voltage levels, the POL converters can be synchronous buck or synchronous boost to give the greatest efficiency. Finally, the controllers can also be simple to enable the smallest size. The next issue is which voltage level, for the distributed bus, will give the optimum efficiency for the complete system. This distributed bus forms the input for the POL converters; and, for instance, if 12 V is selected, then a higher-V_{DS} rated MOSFET is needed than would be required if a 3.3 V bus is used.

Below, we discuss the fundamental requirements for the POL and present efficiency results for the most efficient solutions. Integrated solutions are concentrated on, as they are becoming the ideal solution for POL converters to improve power density and efficiency. The paper investigates new integrated driver plus control and synchronous MOSFET solutions, shown in Figure 12. These devices are presented in two sizes (9 mm by 9 mm and 10 mm by 10 mm), with the smaller device being able to handle approximately 20 A and the larger 25 A. Efficiency results are presented for both devices at various operating conditions, in conjunction with the front-end converter.

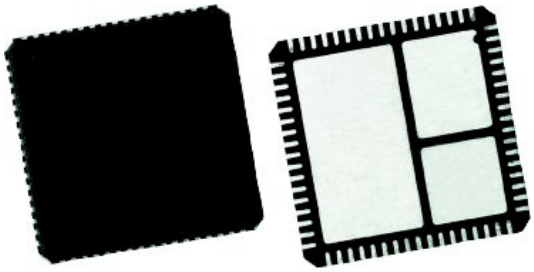

Figure 12. Drawing showing outline of integrated high side, low side MOSFETs and driver.

Sizing Silicon for Specific Applications

The MOSFET requirements in POL converters are very specific for each application. In particular, the silicon requirements for the high-side and low-side MOSFETs are completely different, and choosing the correct silicon has a large impact on efficiency. Scaling procedures can be used to help designers to determine the most apt silicon for their applications.

A typical POL synchronous buck converter operation condition, consisting of a 12-V input and a 1.5-V output, results in a duty cycle requirement that could be as low as 12.5%. This dictates the physical size of the silicon for the high-side and low-side devices. The size of the silicon for the low-side device needs to be large enough to provide a small $r_{DS(on)}$, whereas the high-side device should be small enough to enable faster switching times and hence smaller switching losses. There are other POL applications, where the input voltage is closer to the output voltage, resulting in higher duty cycles. In these cases, the size of the silicon for both devices needs to be very similar. Therefore, for a given process technology, MOSFET cell density, and specific available area of silicon, it is best to scale the high-side switch and low-side switch accordingly. Figure 13a shows an analysis of a synchronous buck converter with a 12-V input and a 1.5-V output and how the efficiency varies with different die size ratios between high-side and low-side MOSFET, where the x-axis is the ratio of silicon for a specific given total area. In this case the die size ratio is defined as being normalised to the low-side device silicon. As the die ratio increases, switching losses become dominant and progressively reduce efficiency. As the die ratio decreases, conduction losses tend to drive the efficiency lower. The optimum high-side-to-low-side silicon ratio in terms of efficiency for this case is 0.5:1.0. Figure 13b shows the same analysis for the same amount of total silicon area, but with a higher input voltage level of 20 V. In this instance the ideal ratio of high-side silicon area to low-side is 0.3:1.0. By knowing this, it is possible to maximize the low-side silicon area for the appropriate current level and then scale the high-side device area accordingly. For high duty cycle applications, such as POL converters with low input voltages, the ideal die ratio is 1.0:1.0.

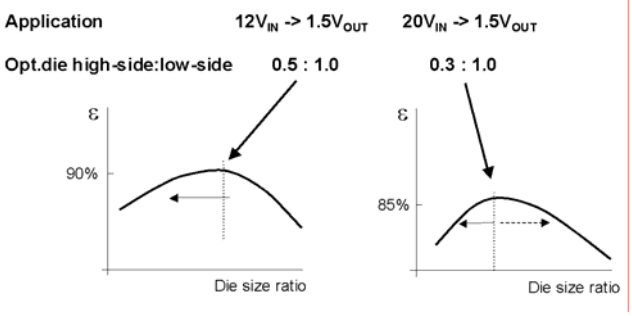

Figure 13. Effect of die ratio on efficiency.[4]

Therefore it is possible to obtain extremely efficient POL converters by sizing the silicon for the specific application. The efficiencies of two different integrated devices designed for low duty cycles and medium duty cycles are shown in Figures 14 and 15 respectively.

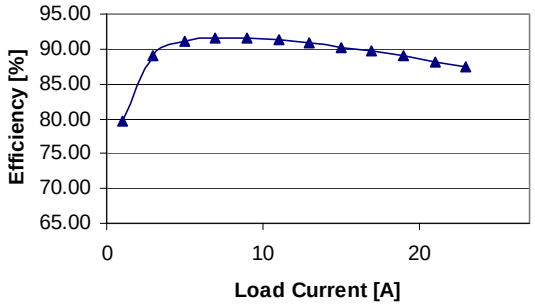

Figure 14. Efficiency results for Integrated Driver and MOSFETs (SiC710CD) designed for low duty cycles < 30%. (12Vin and 2.5Vout)

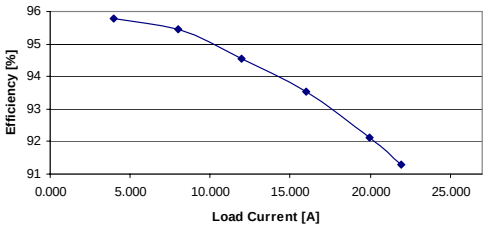

Figure 15. Efficiency results for Integrated Driver and MOSFETs (SiC711CD) designed for duty cycles greater than 30% (5Vin 3.3Vout)

Conclusion

The paper has shown that there are several factors which need to be considered when choosing the voltage level for an intermediate bus. However, for any voltage level chosen it is possible to manipulate the circuitry to increase efficiency. It is probable that once the requirements for 3.3-V loads subside, then the intermediate voltage will be higher. As can be seen in table 3, the total losses for a four-phase solution, using analytical equations[5], the total loss for the 40-A load is less with the 5-V bus.

Lower voltage outputs mean higher load currents and more losses for the same power levels, but a 3.3-V distributed bus does have the advantage of already having the 3.3-V output available. Also, the efficiency can be dramatically improved with synchronous rectification, which may not be the case with the higher-output voltage converter. This is possible since the intermediate voltage allows the voltage regulation to be achieved at the POL converter, and as such the distributed intermediate voltage does not necessarily need to be a fixed voltage.

	Vin		
Load [A]	**12V**	**5V**	**3.3V**
Conduction Losses			
10	0.17	0.19	0.21
20	0.73	0.82	0.91
30	1.80	1.99	2.25
40	3.63	3.96	4.63
Switching Losses			
10	1.77	1.26	0.60
20	2.64	1.63	1.38
30	3.51	1.99	1.62
40	4.38	2.35	1.86
Total losses			
10	1.94	1.46	0.81
20	3.37	2.44	2.29
30	5.31	3.98	3.87
40	8.01	6.31	6.48

Table 3. Losses calculated using analytical equations[5]

References

1 'Si9118/9 demonstration board', http://www.vishay.com/docs/70875/70875.pdf.

2 'Designing a high-frequency, self-resonant reset forward DC/DC for telecom using Si9118/9 PWM/PSM controller', AN724, http://www.vishay.com/docs/70824/70824.pdf .

3 'High efficiency half bridge DC to DC converter with secondary synchronous rectification', Brown, Davies, Williams, Bernacchi, PCIM 2001, June 19-21, Nuremberg, Germany

4. ‘MOSFETS ASM Integrated Circuit – Dr MOS’, Derek Koonce, Jacek Korec, Peter Dang, and Jasper Hou, 2nd Int. PCIM Conf. Shanghai, China, March 2003.
5. ‘Improving the performance of Power MOSFETs by tailoring the driver to the specific MOSFET gate requirements’, Jess Brown, Derek Koonce, Jasper Hou, Nuremberg Germany, PCIM 2003.